

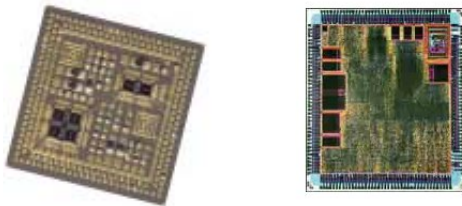
# Jazz Semiconductor RFIC technologies enable advanced RF SiP designs

David Cheskis – Jazz Semiconductor

## Introduction

Jazz Semiconductor has developed Si CMOS and SiGe BiCMOS technologies that change the way that communications systems are designed and partitioned. Jazz now offers several different technology modules that enable the analog partition of a system to include high speed, high performance and high voltage blocks in analog integrated components as part of a System-in-Package (SiP) configuration.

The System-in-Package (SiP) approach offers an alternative to the challenges involved with integrating both analog and digital functions into a System-on-Chip (SoC) design. The SiP approach allows the system designer to implement the analog and digital partitions into technologies optimized for those unique functions. The digital components can be integrated into high performance CMOS while the analog and RF blocks are implemented in lower cost, high voltage and RF CMOS and high performance SiGe BiCMOS. Implementations of the SiP and SoC are shown below and demonstrate the die size and integration requirements.



SiP vs. SoC

Jazz technologies are compatible with the Cadence RF SiP Methodology Kit and enable the system designer to optimize the cost and performance trade-offs necessary for high volume communications products. The Cadence RF SiP flow affords the system designer the opportunity to improve the system performance by optimizing individual components and including the effects of the package or substrate. This chip and package co-development is a significant advance in the design and implementation of communication ICs.

## Jazz Analog IC Technologies

Jazz continues to develop technologies that promote analog integration of system functions, including Si CMOS and SiGe BiCMOS from 0.5  $\mu\text{m}$  to 130 nm, complete with high voltage operation up to 8 V. This allows for advanced integration of power management and other high voltage circuits onto the same system partition as high speed, high performance analog functions. Shown below in Table 1 are the Jazz analog technology modules.

Technology Node	Available Technologies
0.5 $\mu\text{m}$	CMOS, RFCMOS, BCD
0.35 $\mu\text{m}$	60 GHz SiGe BiCMOS
0.25 $\mu\text{m}$	CMOS, RFCMOS, HV CMOS
180 nm	CMOS, RFCMOS, HV CMOS 90/120/200 GHz SiGe BiCMOS
130 nm	CMOS, RFCMOS 100/150/200 GHz SiGe BiCMOS

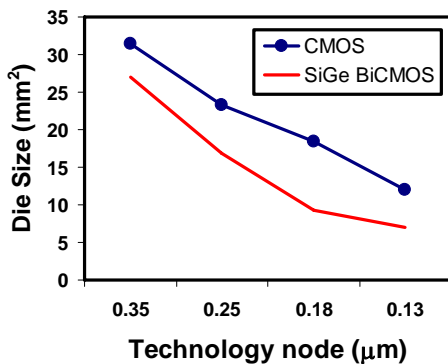
These extensive analog technology offerings enable integration of diverse components such as transceivers, amplifiers, ADC and power management into the analog partition of the system.

Highly efficient analog integration is also facilitated by the advanced passive elements in the Jazz technology. High density MIM capacitors, high Q inductors and triple n-well processes all allow for more compact designs at high speeds with improved performance. Each of these elements can be utilized where appropriate for cost and performance requirements as a result of the Jazz modular technology approach. Table 2 shows some of the passive element modules that are available in the Jazz technologies.

Device	Feature
MIM capacitor	5.6 fF/ $\mu\text{m}^2$
Inductor (Q @ 2.4 GHz)	>15
Inductor thickness	3.0 – 6.0 $\mu\text{m}$

With all of these pieces of the analog puzzle, Jazz has consolidated analog technologies that provide technology solutions for analog integration in one specialty foundry. This approach complements the advanced CMOS processes at 130 nm and 90 nm which are ideal for highly integrated digital functions. While these digital processes are capable of analog integration, they are not as cost effective, or of comparable performance, as 180 nm RFCMOS or 180 nm SiGe BiCMOS. Jazz technology is complementary to advanced CMOS when a SiP design approach is applied, using analog and digital domains optimized in the Cadence RF SiP Architect tool.

Using the SiP approach provides optimized die scaling because the analog functions can be scaled better in a process with high performance passive elements and RF components. The following graph shows the die size for various technology nodes, assuming nearly equal digital and analog content. The impact of analog scaling, including highly integrated passive devices, is to reduce the SiGe BiCMOS chip size compared to a digital CMOS implementation by 20 – 50 %.



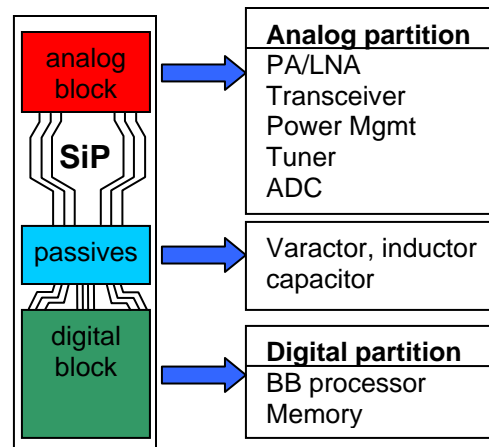
### The SiP Approach

The System-in-Package (SiP) approach to system design is becoming more important as larger sections, and more functionality, become integrated into one product. As additional features are integrated into one IC, it becomes more difficult to accomplish that integration with a single technology, as in the System-on-Chip (SoC) design. The SiP allows for the system to be partitioned into separate analog and digital functions, so that each can be optimized separately for

best performance. One key advantage is that effects of noise from the digital blocks can be effectively minimized and controlled. Another is the ability to integrate additional passive devices into the package for higher performance and lower cost. At the same time, the SiP provides the best IC cost structure because all of the analog blocks don't need to consume expensive 90 nm CMOS real estate. This also results in smaller die size and lower power dissipation. The Cadence RF SiP methodology is a key to effective SiP design optimization.

The SiP approach also allows the designer to take full advantage of both increased digital density and analog scaling. Advanced digital CMOS scales according to Moore's Law; increasing the digital density by approximately 50% in each generation. Unfortunately, the analog and passive devices do not achieve similar performance improvements in subsequent CMOS generations. The Jazz technology roadmap has aggressively scaled the analog components (MIM, inductor, etc.) to remedy this. System partitioning allows the designer to utilize the appropriate analog technology for each block to achieve analog scaling.

An example of SiP partitioning is shown below. A typical wireless system includes RF/analog blocks such as the PA, LNA, VCO, PLL, ADC, integrated passives and power management. The digital partition includes baseband processing, memory, camera processing and other digital functions.



SoC designs require expensive, advanced CMOS technologies to integrate analog

functions into digital blocks in digital processes. Mixed-signal designs with large analog content are difficult to implement in technologies developed for large digital chips. The SiP approach allows for analog and RF blocks to be designed into lower cost CMOS and BiCMOS which are better suited for RF performance and are lower cost technologies. In addition to providing less cross-talk than in a SoC, the BiCMOS module allows designers to capitalize on the low noise performance of the HBT. Typically, analog performance that requires 90 nm CMOS can be achieved in 180 nm BiCMOS at smaller die sizes and lower die cost.

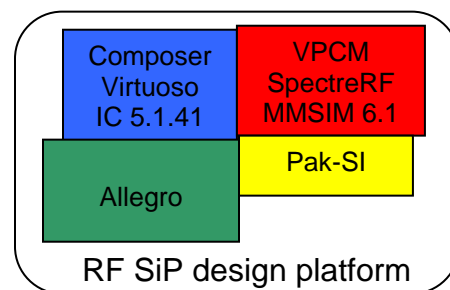
Using the proper digital technology also allows the IC designer to optimize the power dissipation of large digital blocks. When forced to utilize a digital technology that provides analog performance, designers are at the mercy of high leakage currents, high stand-by power and high power consumption. This can be mitigated in the SiP by choosing the appropriate technology for the digital sections without concern for the analog/RF performance.

Another important issue in SoC design is thermal management. In order to accommodate the analog and digital functions on one SoC chip, the die sizes have grown very large and present significant thermal challenges. By partitioning the system in the SiP, the thermal requirements of each chip can be addressed individually. This provides lower package cost and better reliability in the SiP implementation.

Even though all of these design constraints are managed in a SoC, the system designer still needs to be concerned with the package cost and performance. Using the Cadence RF SiP design flow, the SiP designer can determine the effects that the package and substrate will have on product performance. This platform allows the designer to control all aspects of the system performance, including where it is most efficient to partition the system between the analog and digital domains. This control over the ultimate system performance improves the yield and manufacturability of these

advanced, highly integrated communications systems products.

The Cadence RF SiP Methodology Kit is comprised of an integrated set of design tools to allow the system designer a more accurate implementation of the SiP. The Cadence RF SiP Methodology Kit includes the standard Cadence IC design, simulation and layout tools along with the standard Cadence package layout, simulation and signal integrity tools. The components included in the Cadence SiP Methodology Kit are shown below. This provides a SiP design flow in a single tool that does not require an expert user, allows more accurate system simulation and provides faster time to market.



In addition to the right combination of technologies for analog integration, Jazz enables this SiP approach by providing advanced modeling and design kit implementation. Because the Jazz technologies are designed for analog and RF applications, the devices and models are optimized for RF performance. That includes the layout p-cells, extraction and simulation capabilities. Jazz also has built-in AssuraRF support for substrate modeling, which is important for understanding noise and isolation within a design.

The Cadence RF SiP Methodology provides the design platform to tie all of this system optimization together by including the packaging materials and PCB properties into the system design. Jazz fully supports the MMSIM 6 platform for system simulation and plans to provide support for multi-technology simulation when that is available in IC6.1.

**Conclusion**

The SiP design approach is a more cost effective system solution than the SoC. It allows the designer to choose technologies optimized for specific analog functions that are lower cost than a SoC implementation. This system partitioning also allows for shorter design cycles because each block utilizes the optimum technology, leading to lower development costs and faster time to market.

Jazz provides the technologies needed for analog functional integration in advanced communications systems. With high speed and high voltage modular technology offerings, most of the analog functions can be optimized on a single analog IC.

The Cadence RF SiP Methodology Kit enables SiP modeling to achieve optimum system performance, including the effects of the package, PCB, integrated passive devices and system partitioning. Jazz technologies are compatible with the Cadence RF SiP flow and allow the system designer to take full advantage of analog integration and system partitioning.