

**October 22, 2008**

**Newport Beach,  
California**



**Analog-Intensive Mixed-Signal**

**AIMS**

**CAT**

**Circuits, Applications & Technology**

**Jazz** is pleased to offer the **AIMS-CAT Conference** which brings together a wide range of influential technical professionals and managers focused on analog-intensive mixed-signal circuits, applications, and technology to discuss the latest trends and results

# AIMS-CAT Conference Agenda

**Wednesday, October 22, 2008**

- 11:00 **Registration**
- 11:30 **Opening Remarks**
- 12:00 **Lunch/Tables Open**
- 12:45 **Fab Tour available**
- 1:30 **Breakout Session I and II**
- 3:30 **Break**
- 3:45 **Breakout Session III and IV**
- 6:00 **Welcome**
- 6:15 **Happy Hour/Tables Open**

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## Opening Remarks

**Marco Racanelli, PhD** — *VP Technology & Engineering, Aerospace/Defense General Manager for Jazz Semiconductor*

Dr. Marco Racanelli leads technology development, modeling, design automation and design service teams at Jazz. Previously, he held positions with Conexant and Rockwell Semiconductor Systems, helping to establish industry leadership in SiGe and BiCMOS technology. Prior to Rockwell, he worked at Motorola where he contributed to bipolar, SiGe and SOI development. He holds over 30 U.S. patents and has authored or co-authored more than 40 technical publications.

## Breakout Session I

### 1. High-Performance BiCMOS Microwave and Millimeter-Wave Phased Arrays

**Gabriel Rebeiz, PhD** — *Professor, University of California San Diego*

This talk will present microwave and mm-wave phased arrays covering distinct frequency bands, from 2GHz to > 60GHz, using the Jazz SiGe18HX processes. The results show state-of-the-art performance, and the work is done at the RF level leading to conceptually very simple designs which have a very wide bandwidth. Typical designs include an 8-element 8–16GHz SiGe phased array receiver, a 16-element 35–50GHz SiGe transmit phased array, and a miniature (< 5mm<sup>2</sup>) 4-element BiCMOS phased array transceiver at Ka-Band frequencies. Application areas are satellite communications, defense systems, imaging systems, and automotive radars.

### 2. 24GHz UWB front-end BiCMOS ICs for Short-Range Automotive Radar

**Hugo Veenstra, PhD** — *Philips Research Laboratories*

Short-range radar is a technology that can help to enhance road safety. Recently, in the USA as well as in Europe, frequency bands around 24GHz have been opened up for automotive radar applications. This paper describes Ultra-Wideband (UWB) transmitter and receiver ICs realized in a production 0.25µm SiGe BiCMOS IC technology. The UWB signal is generated by means of biphasic modulation of a 24GHz carrier with a pseudo-noise data signal. The transmitter IC generates a maximum unmodulated output power of 5dBm for frequencies between 15–27GHz. The quadrature receiver IC achieves an NF of <7dB across a 2.5GHz IF bandwidth.

### 3. Complex Millimeter-Wave SiGe IC – 24GHz Automotive Radar

**Nitin Jain, PhD** — *CTO, Anokiwave*

Anokiwave has successfully designed what has been dubbed “one of the most complex mm-wave (MMW) SiGe ICs to-date” for a 24GHz Automotive Radar application in Jazz’s SBC18HA process. The IC contains a complete PLL, two receivers at 24GHz, a 24GHz transmitter, monotonic 15-bit DAC, voltage regulators, instrumentation quality opamps and comparators with an integrated SPI bus, and ESD protection. All this was achieved with exceedingly good noise.

In addition to the functional complexity, the project also had a demanding schedule of design time of 9 months. Thanks to thorough design methods and excellent Jazz models, Anokiwave succeeded in achieving first pass success and ensured that their customer, U.S. Monolithics, were able to target the market opportunity. The entire chip occupied an area of 2.7mm by 2.7mm. In this presentation Anokiwave will provide an overview of some of the subcomponents that it has successfully designed.

#### **4. A Novel Millimeter-Wave Transceiver for Automotive Radars in Jazz BiCMOS Technologies**

**Payam Heydari, PhD** — *Associate Professor of Electrical Engineering and the EECS Associate Chair for Graduate Affairs, University of California, Irvine*

The proliferation of various mm-wave (MMW) frequency bands allocated by the Federal Communications Commission (FCC) has enabled new generations of short- and long-range automotive radar sensors. MMW automotive radars have mostly been implemented in fast, expensive III-V compound semiconductor technologies as monolithic microwave integrated circuits (MMICs). This is primarily because of the extremely high frequency of operation mandated by these radar transceivers. Recent advances in silicon (Si) and silicon-germanium (SiGe) technologies have made it possible to design silicon-based MMW integrated circuits. In this talk, design/fabrication/measurement of the first dual-band MMW transceiver for automotive radar applications in Jazz's SBC18 process is presented.

### **Breakout Session II**

#### **5. Recent Benchmark Results with Virtuoso RF Designer and Several RF Process Design Kits from Jazz Semiconductor**

**Sutirtha Kabir** — *Staff Product Engineer, Custom IC Design, Cadence Design Systems*

Various types of parasitic for an IC have a first-order impact on RF circuit performance. Additionally, high density layout and GHz range operating frequencies introduce numerous high frequency effects including time retardation, the skin effect, substrate effects, and harmonic resonances. To overcome these obstacles, it is essential to accurately predict parasitics and high frequency effects while designing RFICs. Unlike traditional flows, Cadence® Virtuoso® RF Designer delivers a comprehensive electromagnetic (EM) simulation and verification solution. By simultaneously considering electrical and physical effects, it reduces iterations between layout and schematic. This paper presents results from a recent benchmark with Virtuoso RF Designer and several RF PDKs from Jazz.

#### **6. Early Substrate Isolation in Mixed-Signal Devices**

**Venkat Ramasubramanian** — *Sr. CoreComp Technical Leader, Cadence Design Systems*

As high levels of integration are required for mixed-signal ICs, designing sensitive high frequency RF and analog blocks on the same die as noisy digital circuits is unavoidable. Isolation becomes critical in this scenario and

designers must determine feasible noise isolation techniques and enable early prediction of possible spur problems. To address substrate isolation, a methodology is needed that enables early predictions to improve accuracy incrementally to meet simulation goals. This session describes components in this methodology from the technology setup of a 0.18 $\mu\text{m}$  SiGe BiCMOS process, the substrate extraction with Cadence QRC to compare to silicon measurements on test structures, and finally, the application of substrate extraction to a full-chip floorplan, representing a realistic scenario to study isolation strategies and perform what-if analysis using noise contour maps.

## **7. Analog/Mixed Signal ASICs Using Via-Configurable Arrays**

**Jim Kemerling** — *CTO, Triad Semiconductor, Inc.*

As the minimum feature size of semiconductor processes shrink, tooling costs escalate. Moreover, smaller minimum feature size leads to higher gate counts. Consequently, full-custom designs using smaller geometry processes ( $\leq 0.35$  micron) cost more and take longer to design. It is difficult, for even the largest companies, to justify investment in analog or mixed signal full-custom ASICs. Via-Configurable Arrays (VCAs) provide a low cost, quick turn alternative.

Analog IC design has long been considered "full-custom only." In this presentation we will introduce via-configurable analog/mixed signal technology as a means for resolving many of the issues confronting analog/mixed signal IC designers — cycle time and tooling cost. We will show how VCAs are developed and how they are configured using a single via layer. In addition, we will show how the VCA design process works and how VCA technology provides a path to full-custom solutions with much lower risk and lower overall cost.

## **8. Statistical Modeling with the PSP MOSFET Model**

**Xin Li** — *Graduate Research Assistant, Arizona State University*

PSP is the next generation standard MOSFET model. The strong physical content of PSP provides a sound basis for statistical modeling. PSP and the Backward Propagation of Variance (BPV) method are used to characterize the statistical variations of MOSFETs. BPV statistical modeling of NMOS and PMOS devices is, for the first time, coupled by including self-consistent modeling of ring oscillator gate delays. Parasitic capacitances are included in the analyses. The proposed technique is validated using Monte-Carlo simulations and by comparison to experimental data from two technologies.

## **Breakout Session III**

## **9. Performance and Modeling of Si and SiGe for Power Amplifiers**

**Peter Zampardi** — *Technical Director, Skyworks*

There have been many demonstrations of Si and SiGe power amplifiers (PAs) that have achieved good published performance. However, penetration of these technologies into the mainstream handset power amplifier market has been limited. In this paper, we review some of the state-of-the-art PA results in these technologies and discuss the performance challenges for silicon-based

PAs. We also discuss some important on-going technology developments that may make these technologies more competitive for future applications. Finally, we present and discuss some power amplifier specific modeling issues that are not generally addressed in foundry offerings/design kits.

## **10. MEMS Resonators for High Speed and Low Phase Noise Applications**

**Paul Hagelin** — *Director of MEMS Engineering, SiTime*

Electronic innovations continue to demand greater performance at smaller scales. At the heart of almost every circuit is a clock. Partnering with Jazz, SiTime has created a MEMS silicon resonator to replace bulk quartz crystals. The knowledge gained in producing and shipping the first generation device has enabled the development of a next generation resonator with higher frequency and lower noise. With Jazz optimization of the fundamental etch process that forms the resonator, SiTime has been able to create a new class of high frequency resonators with greatly improved performance.

SiTime's latest design has a fundamental frequency of 48MHz vs. 5MHz in the first generation. By leveraging the new etch and doubling the substrate thickness, this new resonator design is even more robust. Careful compensation of the design has reduced the variation in the fundamental frequency by a factor of 10 over process. Furthermore, the phase noise has improved by 20dB in going from 5MHz to 48MHz. These advances open the door for MEMS resonators in applications that require high data rates with low jitter or phase noise.

## **11. Monolithic RF-MEMS on CMOS for Commercial Wireless**

**Art Morris** — *CTO, WiSpry*

Commercial wireless applications continue to diversify leading to an increasingly unwieldy set of RF hardware implementations and design compromises. These limitations increase the size of each platform, limit the performance and lengthen the design cycle. Adding enablement to RF front-end elements is a key enabler to reversing this trend and providing a flexible platform for tomorrow's systems. WiSpry has teamed with Jazz Semiconductor to develop a high-performance tunable RF capability based on RF-MEMS monolithically integrated with mixed-signal CMOS for digital control. Prototype performance will be presented for arrays of tunable capacitors and tunable circuits.

## **12. An Integrated, Tunable RF Filter: An Enabler for Reconfigurable Front-Ends**

**Tom Riley** — *CTO, Kaben Wireless Silicon, Inc.*

This paper presents the design and performance of a key RF circuit necessary for the realization of a reconfigurable, integrated RF front-end: a tunable frequency, selectable bandwidth, on-chip, "SAW replacement" filter. The on-die tunable filter presented here has a tunable center frequency up to 1GHz, a selectable bandwidth up to 40MHz, and an adjacent channel rejection down to 60dB.

## Breakout Session IV

### 13. A 10Gbps Adaptive Loop Bandwidth Clock and Data Recovery with On-Chip Loop Filter

**Jose Silva-Martinez, PhD** — Associate Professor, Texas A&M University

Since incoming jitter cannot be predicted in advance, optimizing the loop by adjusting the bang-bang bandwidth adaptively to minimize CDR's steady state jitter leads to an improved jitter tolerance performance. Complete architecture of the proposed adaptive bang-bang CDR will be presented. Bandwidth adaptation technique will be highlighted along with implementation details of critical building blocks. Behavioral simulations in support of improved jitter performance and transistor level simulation results for the building blocks using Jazz-SiGe BiCMOS 0.18 $\mu$ m technology will be included.

### 14. Back-Illuminated CMOS Image Sensor Technology

**David Cheskis, PhD** — Business Director, Sarnoff Corporation

Back-illuminated CMOS image sensors are becoming more commonplace in high-performance imaging systems, given the inherent benefits when compared to their front-illuminated counterparts. However, their increased manufacturing complexity and high costs have constrained them for use in higher-end systems.

Recently, a breakthrough combining novel material technologies and fabrication processes has been achieved that will make back-illuminated imagers readily available for mass production. This paper presents the Sarnoff Ultra-Sense™ solution using ultra-thin silicon-on-insulator wafer technology to reduce the manufacturing complexity and effectively solve the cost-performance challenge for high performance imagers. This enables back-illumination in applications from Deep UV inspection systems to high resolution consumer electronics.

### 15. OTP for Security, Calibration, and Configuration

**Steve Warner** — VP Marketing, Novocell

Now available in standard CMOS, one-time programmable (OTP) memory can provide added capabilities to any IC design. Security keys can be locked into a device to prevent its unauthorized use. Other ICs may benefit from the use of OTP to adjust out offsets or process variations in analog circuitry. Often times an IC is destined for use by multiple customers and selecting options and custom features can be done by OTP configuration registers. The OTP memory can be easily interfaced to other on-chip circuitry, and the OTP memory can be programmed at wafer, final test, or during operation in the target application.

### 16. A 25MHz Bandwidth 12-Bit Continuous-Time Low-Pass $\Sigma\Delta$ Modulator Design in Jazz 0.18 $\mu$ m CMOS Technology

**Jose Silva-Martinez, PhD** — Associate Professor, Texas A&M University

The design of a 12-bit continuous-time low-pass sigma-delta modulator with 25MHz bandwidth will be discussed. A novel multi-phase feedback digital-analog-converter (DAC) concept is presented to overcome non-linearity

problems of multi-bit DACs together with an injection-locked frequency divider for clock generation. Additionally, calibration is performed with injection of two tones outside the signal bandwidth for performance optimization under the influence of variations. Behavioral system simulations of the architecture resulted in a 73.8dB SQNR.

## Speaker Biographies

### David Cheskis, PhD

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Dr. David Cheskis serves as Business Director at Sarnoff Corporation and is responsible for leading technology commercialization in the Imaging Systems division. Since joining Sarnoff, he has led the introduction of the Ultra-Sense™ solution for back-illuminated image sensors. Dr. Cheskis has worked over the last 10 years on semiconductor technology and product development.

### Paul Hagelin

Title: Director of MEMS Engineering  
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Paul has thirteen years of experience in MEMS (micro-electromechanical systems). At SiTime, Paul's team develops resonators for silicon timing applications and partners with Jazz to produce them. Previously, Paul co-founded C Speed Corporation, where he directed the MEMS Engineering group in the development of an optical cross-connect switch.

### Payam Heydari, PhD

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Dr. Payam Heydari serves as the Associate Editor of *IEEE Trans. on Circuits and Systems - I*, and the Guest Editor of *IEEE Journal of Solid-State Circuits*. He currently serves on the Technical Program Committees of Custom Integrated Circuits Conference (CICC), ISLPED, and International Symposium on Quality Electronic Design (ISQED).

### Nitin Jain, PhD

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Dr. Nitin Jain is CTO of Anokiwave, Inc., where he is consulting and designing circuits for various customers. His current interests include mm-wave circuits, mm-wave modules, Silicon and GaAs MMIC circuits, EM simulations, and passive circuit modeling and design. He has authored over 20 publications in international conferences and journals and has six U.S. patents.

### **Sutirtha Kabir**

Title: Staff Product Engineer, Custom IC Design  
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Sutirtha Kabir is a Staff Product Engineer at Cadence Design Systems and works with a new product called Virtuoso RF Designer, a planar electromagnetic full-wave field solver. He came to Cadence through the Neoliner acquisition and previously worked at the Semiconductor Products Sector at Motorola, which later became Freescale Semiconductor.

### **Jim Kemerling**

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Jim Kemerling, a founder and CTO of Triad Semiconductor, is responsible for VCA technology development and implementation. He has over 23 years of experience with semiconductors and system-level design. Before starting Triad Semiconductor, he gained experience with hands-on R&D management positions at market-leading companies, including MX-COM, General Electric/Ericsson, and Rockwell International.

### **Xin Li**

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Xin Li received the B.S. degree from Huazhong University of Science and Technology, Wuhan, China, in 2001, and M.S. degree from The Pennsylvania State University, University Park, in 2006, both in electrical engineering. He is currently working toward his PhD degree in electrical engineering at the Arizona State University. Xin Li is a member of the joint ASU/NXP development team of the PSP model.

### **Jose Silva-Martinez, PhD**

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Dr. Jose Silva-Martinez is with the Department of Electrical Engineering, Texas A&M University, in the position of Associate Professor. His current research is on IC design. He's the inaugural holder of the TI Professorship-I and recipient of the 2005 Outstanding Professor Award ECE Department and co-recipient of several awards.

**Art Morris**

Title: CTO

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Dr. Art Morris is CTO and co-founder of WiSpry, Inc., developing programmable RF circuits for commercial wireless applications. Art has focused on physical electronics and electromagnetics for over 25 years working with applications from power systems through optical communications. Dr. Morris is a Senior Member of IEEE and an adjunct professor at NCSU.

**Venkat Ramasubramanian**

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Venkat Ramasubramanian received a Masters in Electrical Engineering from Stanford University. Before joining Cadence, Venkat worked as an applications engineer at Simplex Solutions where he was mainly supporting the substrate extraction solutions. Since joining Cadence in 2002, Venkat has continued supporting this specialized technology both with customers as well as internally working with the product development groups to architect new interfaces and methodologies for improving the capabilities of substrate extraction and analysis solutions.

**Gabriel Rebeiz**

Title: Professor ECE Department

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Gabriel Rebeiz (Fellow, IEEE) is a Professor of electrical and computer engineering at the University of California, San Diego. Professor Rebeiz's group developed 6–19GHz and 30–50GHz phased arrays using the Jazz SBC18HX process. Professor Rebeiz is an NSF Presidential Young Investigator, and is the recipient of the 2000 Microwave Prize. He is the Director of the *UCSD/DARPA Center on RF MEMS*.

**Tom Riley**

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Tom Riley is CTO and founder of Kaben Wireless Silicon. He is a prolific inventor and holds many patents in the area of mixed-signal RF design. Past positions include a variety of R&D and advanced engineering functions with Nortel Semiconductor, Mitel Semiconductor, Gennum, CAL, Conexant, and as a research engineer with Carleton University.

**Steve Warner**

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Steve Warner joined Novocell in May 2007 to head up the company's sales and marketing strategy, drive product commercialization, and manage its business operations. Mr. Warner is a seasoned executive with 30 years of business experience in power storage manufacturing, operations, finance, and business development.

**Hugo Veenstra, PhD**

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Hugo Veenstra was born in The Netherlands. He received his PhD degree in Electrical Engineering from the Delft University of Technology in 2006. In 1992 he joined Philips Research Laboratories where he has been involved in analog, mixed-signal and mm-Wave IC design for transceiver applications.

**Peter Zampardi, PhD**

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Dr. P.J. Zampardi, B.E. received his degree in Engineering Physics from Stevens Institute of Technology in 1986, his M.S. degree from Caltech in Applied Physics in 1988, and his PhD from UCLA in 1997. He has worked in various Rockwell divisions on gyroscopes, optics, and high-speed electronics and also worked on silicon germanium technology at IBM. Since 2001, he has been at Skyworks Solutions where he is the Technical Director for the Newbury Park Technology Development Group. The Group's interests are technologies, characterization, modeling, and circuit design for wireless applications, especially power amplifiers.



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