AIMS-CAT Conference
November 5, 2009 – Newport Beach, CA

TowerJazz is pleased to offer the AIMS-CAT conference which brings together a wide range of influential technical professionals and managers focused on analog-intensive mixed-signal circuits, applications, and technology to discuss the latest trends and results.

Conference Agenda

1:30 AIMS-CAT Breakout Session A and B
2:00 AIMS-CAT Breakout Session C and D
2:30 AIMS-CAT Breakout Session E and F
3:00 Afternoon Break
3:15 AIMS-CAT Breakout Session G and H
3:45 AIMS-CAT Breakout Session I and J
4:15 AIMS-CAT Breakout Session K and L
4:45 Wrap-up
5:00 Giveaways – in sponsor tent
5:15 Happy Hour with appetizers – in sponsor tent
7:30 Event ends

Join us and experience the latest with tool and IP providers, design companies, and post wafer service companies at the sponsor tables located in the Suppliers Tent.

1:30 pm

Breakout Session A

Emerging Millimeter Wave Applications Driving Needs for Higher Process Performance
By: Ramesh Ramchandani, TowerJazz, Newport Beach

As the millimeter wave continues to grow with emerging applications, the need for higher performance process technologies is becoming more and more prevalent. For example, the need for Silicon capability with the ability to drive logic integration necessitates higher speed SiGe in many commercial applications including collision avoidance radar, 60GHz commercial WLAN, optical networking in both access and central office requiring higher data rates, and even some commercial phased array applications. This presentation will focus on markets and technical solutions being addressed in the millimeter wave emerging applications.

Breakout Session B

Integrated Power Management Platforms: Requirements for Foundry Process Offerings

By: Avi Strum, TowerJazz, Migdal Haemek

We will discuss a complete family of process offerings which address the broad needs of the integrated power management platforms market. For instance, one of our process technologies integrates a 0.18-micron analog and digital platform with power devices scalable in voltages up to 80V, maintaining an optimal Rdson breakdown voltage tradeoff. We also offer a patented self-aligned LDMOS which achieves low Rdson values. In addition, our zero mask adder (digital) non-volatile memory (NVM) solutions are offered along with special buried layer and deep trench options. On the other edge of the voltage axis, we are developing 700V platforms to support 220-240V European grid applications, primarily lighting.

2:00 pm

Breakout Session C

High Performance Two-Antenna Quad-Beam X to Ku-Band Phased Arrays for Satellite and Point-to-Point Communications

By: Dong Woo Kang and Gabriel Rebeiz, University of California, San Diego

The talk will present designs capable of delivering multiple beams at X and Ku-band frequencies with high isolation (Jazz SiGe18Hx). The chips result in a measured gain of 5-6 dB at 14-15GHz, a noise figure of 10-11 dB, a P1 dB of -13 dBm per channel (IIP3 of -6 dBm), and with a 4-bit phase control. A gain control of 17 dB is present at each channel. The on-chip beam-to-beam isolation is >30 dB. The beams can operate over an instantaneous bandwidth of >1GHz at 11-15GHz.

Breakout Session D

Non-Volatile Memory for a Bipolar CMOS-DMOS (BCD) Process

By: Ross Teggatz, Triune Systems

We will discuss the Y-Flash IP small, medium, and large memory modules available in the TS18SLPM process. Embedded NVM offers a cost-effective and programmable flexibility to a power management process. Included topics are the advantages of the Y-Flash memory cell, wrapper architectures for the various sized memory modules, power efficient sense amplifier and charge pump designs, trade-offs within the design between performance and die area, built-in test for quality and observability, and implementation and optimization of error correction codes (ECC) for robust system performance.

2:30 pm

Breakout Session E

TowerJazz Deep-Sub Micron CMOS and RFCMOS Platforms

By: Eitan Shauly, TowerJazz, Migdal Haemek

TowerJazz's advanced 0.13- and 0.18-micron CMOS technologies with high performance and high voltage options are beneficial for large scale integration of mixed-signal ICs. Our mature 0.18-micron platform offers either 1.8/3.3V or 1.8V/5V with up to 6 metals of Al, with FSG or USG, and a large variety of metal options, including fatCu, offering a real 19% area shrink for cost reduction. Our 0.13-micron platform offers up to 8 metal layers and a large variety of metal types, including single or dual fat Cu or Al. Each technology supports multiple Vt and I/O of 2.5V or 3.3V. We will show how our CMOS technology is also the basis for our modular specialty technologies such as Power Management, SiGe BiCMOS, RFCMOS, and others.

Breakout Session F

Current Trends in Imaging Technology

By: Jeff Zarnowski, Panavision Imaging

Imager architecture is evolving to allow wider dynamic range, higher readout speeds, lower noise and greater flexibility. CMOS imagers now have overcome the issues that have made CMOS imagers second rate to CCDs. A combination of improved pixel characteristics as a result of continuous improvement by the foundry and imager architectures that take advantage of the low noise parallel processing CMOS allows. Current state-of-the-art pixel and imager architectures will be reviewed as well as the resulting images and measured data illustrating how CMOS imagers excel over CCDs in image quality.

3:00 pm – Afternoon Break

3:15 pm

Breakout Session G

An 11.1Gbps Analog PRML Receiver for EDC of up to 400km-Reach WDM Fiber-Optic Links

By: Salam Elahmadi, Menara Networks

A dispersion tolerant receiver for fiber-optic links, in 0.18µm SiGe BiCMOS (SBC18HX), implements a Class-2 Partial Response Maximum Likelihood (PRML) equalization entirely in the analog domain. The PRML receiver is capable of post-FEC error-free recovery of up to 11.1Gb/s data transmitted over 400km of uncompensated SMF fiber. The realized reach of this receiver exceeds that of any reported EDC receiver employing standard NRZ transmission and direct detection (non-coherent, IM-DD) means. The outstanding performance of this PRML receiver has been achieved with a 1-sample/bit, 4-state MLSE. To the best of our knowledge this is the first reported analog implementation of the PRML algorithm for a 10Gb/s+ fiber-optic receiver.

Breakout Session H

A Streamlined Design Flow for RF SiGe Applications

By: Chris Mueth, Agilent Technologies

What RF design technology and tools are available to the RF SiGe designers? What are the strengths of the various options available? As SiGe technology continues to make headway into RF applications, designers seek more streamlined and cost-effective design flows using industry leading RF technology. This paper describes a streamlined flow which utilizes the new Jazz process design kits supporting Agilent's Advanced Design System.

An overview of the streamlined RF SiGe design flow will be described as well as the utility of the RF tools utilized. The functionality of the Jazz process design kits will be examined as well as how the kits are utilized in the design flow. The paper will further examine the key applications which utilize this design flow and the design space being addressed.

3:45 pm

Breakout Session I

New Developments in SiGe & CMOS SOI for Wireless Front End Modules

By: Volker Blaschke, TowerJazz, Newport Beach

In this presentation, we give a PA centric overview of Jazz's 0.18µm SiGe and 3.3V/5V thick film SOI process. We will show silicon characterization results on SiGe power amplifier stages. By matching the input of the PAs monolithically on the silicon die, we were able to achieve output power levels that were previously considered the realm of GaAs. A novel ground contact provides a low parasitic ground path with inductances below 5pH for transistor emitter and shunt tuning elements. In addition, we will show RF characterization results on 5V and 3.3V antenna switches for WLAN and cellular handsets.

Breakout Session J

QRC Extraction's Mesh Resistance Computation for Specialized Analog Design Applications

By: Venkat Ramasubramanian, Cadence

Traditional parasitic resistance extraction methodologies involve calculating number of squares as the ratio of length-over-width for interconnect lines. This one dimensional computational methodology is sufficiently accurate for design styles involving long and relatively thin wires where current direction is along the length of the conductor. However in many specialized analog design applications involving power MOS devices, the interconnect shapes around MOS devices are complex non-manhattan planar structures where 1-D resistance computation is not sufficient to model the current paths and crowding effects accurately. The alternative of using Finite Element Modeling (FEM) techniques, though accurate, may not be feasible in circuit-level analysis due to performance limitations.

4:15 pm

Breakout Session K

Load Pull Characterization of SBC18H2 Devices for Power Applications at Millimeter Wave Frequencies

By: Luciano Boglione, University of Massachusetts, Lowell

The load pull measurements of SBC18H2 devices have been performed at Q band for a number of frequencies and bias levels. Load pull data is crucial in understanding and optimizing the power performance of the device, particularly at mm-wave frequencies. This presentation shows the results of our measurements along with a discussion of the load pull setup and the characterization procedure. Comparisons of model vs. measurement are also presented. The information contained in this presentation is not readily available in the Jazz literature and provides useful feedback to SBC18 designers on the power performance of the device at mm-wave frequency.

Breakout Session L

Thermal Gradient and IR Drop Aware Design Flow for Analog-Intensive ASICs

By: Denis Zelenin, Pacific Microchip Corporation

Growing ASICs complexity and speed along with the tightening analog accuracy specifications requires more stringent verification. Two additional design flow steps are presented: 1) die temperature gradient map back-annotation to the netlist, 2) accurate chip-scale simulation of the ground and supply voltage drop.

Thermal gradient impact inclusion in the Spectre simulation enables thermal aware floor planning and accurate prediction of the performance degradation. Accurate IR drop map simulation helps optimize power/ground routing and avoid electro-migration related reliability issues. Presented methodologies utilize standard tools commonly used in IC design flow and were applied for design of PRML-based EDC fiber-optic receiver ASIC.

Speaker Biographies

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Volker Blaschke received the B.S. degree in micromechanics from the University of Applied Sciences, Munich, and the M.S. degree in electrical and computer engineering from the University of Texas at Austin. He is a Distinguished Engineer at Jazz Semiconductor where he manages the SiGe power amplifier technology and RF modeling of passive components.

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Luciano Boglione is assistant professor at the University of Massachusetts, Lowell. He performed this work at the Air Force Research Laboratory, Sensors Directorate, Hanscom AFB MA under the 2009 Air Force Summer Faculty Fellowship Program.

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Salam, founder of Menara Networks, has over 16 years experience in system design, test, and deployment of various communications systems including wireless, wireline, and optical networks. His background combines in-depth knowledge of signal processing techniques, digital communication theory, nonlinear optics propagation, and high-speed electronics.

Chris Mueth
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Chris Mueth currently holds the position of World Wide Business Development Manager at Agilent Technologies, and is active in working to introduce new EDA solutions to address industry trends. Chris has 20 years of experience in R&D management and design in the areas of systems and equipment, integrated subsystems and component design.

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Venkat Ramasubramanian received a Masters in Electrical Engineering from Stanford University. Before joining Cadence, Venkat worked as an applications engineer at Simplex Solutions where he was mainly supporting the substrate extraction solutions. Since joining Cadence in 2002, Venkat has continued supporting this specialized technology both with customers as well as internally working with the product development groups to architect new interfaces and methodologies for improving the capabilities of substrate extraction and analysis solutions.

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Ramesh Ramchandani leads the marketing effort for the RF & HPA business unit for Tower/Jazz Semiconductor. His background includes various management positions in both RF and Power Management companies, including Celeritek, ON Semiconductor, and ZiLOG. He has also held RF design positions in RFIC amplifiers for Avantek and Mitsubishi. He currently serves on the Advisory Board of Arizona State University's School of Engineering and as an advisor to many start up companies.

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Gabriel Rebeiz (Fellow, IEEE) is a Professor of electrical and computer engineering at the University of California, San Diego. Prof Rebeiz's group developed 6-18GHz and 30-50GHz and recently quad-beam 11–15GHz phased arrays using the Jazz process. Prof Rebeiz is an NSF Presidential Young Investigator, and is the recipient of the 2000 Microwave Prize. He is the Director of the *UCSD/DARPA Center on RF MEMS*.

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Eitan N. Shauly received the B.Sc. degree in materials engineering from Ben-Gurion University in 1989, and M.Sc. and Ph.D. degrees in materials engineering from the Technion – Israel Institute of Technology, in 1995 and 2001, respectively. During 1989-1994 he was a diffusion and ion implantation engineer. During 1994-1997 he was a device engineer, focusing on process integration and process modeling. Since 1998 he is doing integration, focusing on platform development, design rules and DFM.

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Dr. Strum joined Tower in December 2004 and served as GM of the design center in Netanya and Device and Integration Department Manager. Subsequently, he was GM of the CMOS sensor and NVM business units. Prior to Tower, he served as the President and COO of TransChip, Inc. and formerly, he was with Intel Corp., serving as the Quality and Reliability Manager of the Processors Division of Intel Israel. Previously, he served as R&D Manager of SCD, in charge of all the Infrared Detectors development. Dr. Strum holds a B.Sc. and Ph.D. in EE from Technion – Israel Institute of Technology.

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Ross Teggatz has 25 years in the IC Design Industry and is recognized as a technical leader. He has served both member and chairman of the IEEE BiCMOS Technology and Circuits Meeting (BCTM), and authored numerous articles and has received over 40 patents. At TI, he held the technical executive position of Fellow.

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Jeff Zarnowski is currently the CTO of Panavision Imaging, LLC. Prior to joining the Panavision team, he served as the CEO and CTO of Silicon Video, Inc., and Founder and CTO of Photon Vision Systems, Inc. He has been in the imaging field since 1985 where he started at General Electric, transferred MOS based CID imagers to CMOS. He has numerous publications in the scientific community as well as numerous imager related patents awarded and pending.

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Denis Zelenin received the B.S. and M.S. degrees in electrical engineering from Vilnius Gediminas Technical University in 1994 and 1996, respectively. From 2000 to 2003, he was with Multilink Technology Corporation as an IC design engineer for high-speed fiber-optics products. In 2003 he joined Pulse~LINK Inc. as a Senior RFIC Designer for ultra wideband products. Since 2006 he is the CTO of Pacific Microchip Corp., Los Angeles, CA, working on ASICs for fiber optics, wireless and imaging applications. His interests include high speed mixed-signal circuits, design and verification methodologies.