

SiGe BiCMOS Technology for Communication Products

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Abstract

SiGe BiCMOS technology is reviewed with focus on recent advances including the achievement of >200 GHz Ft and Fmax SiGe transistors, integration with generic 0.13 μm CMOS, and the realization of low-cost nodes for the integration of wireless transceivers. Record-breaking wireless and wire-line circuit examples are also provided.

Introduction

SiGe BiCMOS is becoming the technology of choice for achieving cost-effective integration in wireless and wireline communication transceivers. Several SiGe BiCMOS technology nodes exist today at commercial foundries ranging in complexity and performance from 0.35 to 0.18 μm geometry and from 60 to 200 GHz Ft (Figure 1).

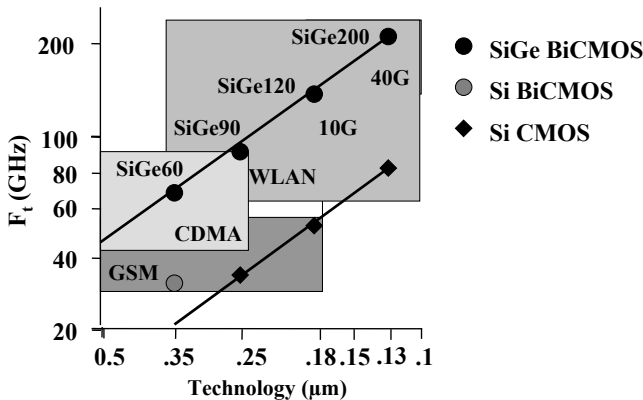


Figure 1. SiGe BiCMOS nodes mapped across major end markets. Plotted as examples are Jazz's SiGe60, SiGe90, SiGe120 and SiGe200 technologies.

In this paper, we will review advances in the performance of SiGe bipolar devices, the integration of these devices with deep sub-micron CMOS, and advances in the realization of high quality passive elements. In the final section of the paper, we will review optimized SiGe BiCMOS technology nodes and discuss performance of benchmark circuits.

High Performance SiGe Bipolar Transistors

Figure 2 shows a cross-section of a state of the art SiGe bipolar transistor. The transistor is built by first forming the buried layer through an implant and subsequent epitaxial growth. Shallow and deep trench isolation elements are then built. Use of deep trench is an option that reduces collector-

substrate capacitance by nearly a factor of 4 for a minimum size NPN but can be removed to reduce wafer cost without impacting other device parameters.

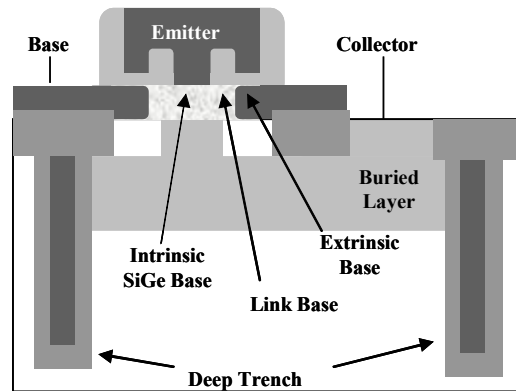


Figure 2: Self-aligned SiGe NPN transistor with deep trench. Self-aligned transistors have intrinsic and extrinsic base formed by a single patterning step leading to a narrow and well controlled link base and low base resistance.

After formation of the CMOS wells, gate, and collector sinker, a SiGe layer is deposited by use of a single wafer RT-CVD reactor.

Next, the emitter is formed. In state of the art technology, the emitter is self-aligned to the extrinsic base resulting in low extrinsic base resistance, high Fmax, and low noise figure. Figure 3 shows the simulated dependence of base resistance at peak Ft on base link width. In a self-aligned device, this dimension can be scaled aggressively (<0.1 μm) while in a quasi-self-aligned (QSA) device this dimension is limited by alignment tolerance. This leads a self-aligned device to have base resistance that is typically 2 times smaller and is better controlled due to the lack of misalignment variation.

In our technology, a sacrificial emitter surrounded by spacers is used to self-align the extrinsic base implant to the emitter (1). The sacrificial emitter is removed and an in-situ doped emitter is deposited such that the dimension of the sacrificial emitter exactly defines the final emitter dimension. This technique leads to the direct patterning of the emitter dimension and thus results in a device that can be scaled more controllably than one employing techniques that rely on inside spacers (2).

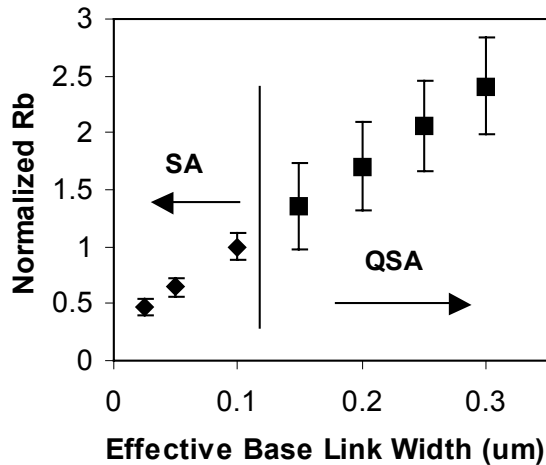


Figure 3: Simulated base resistance (Rb) at peak Ft as a function of base link width. Square symbols assume a quasi-self-aligned (QSA) device and diamonds assume a self-aligned (SA) device. Error bars represent expected 3-sigma variation. Higher and more variable base resistance is typical in a QSA device due to difficulty with scaling and controlling the link base.

This scalable architecture has been employed to build devices with Ft of 35 GHz to over 200 GHz with only small changes to a few process recipes. Figure 4 summarizes some of these results. Ft can be driven from 35 GHz to 150 GHz simply by changing the collector implant condition. Ft can be further increased from 150 GHz to over 200 GHz by changing the collector, and modifying emitter and base profiles. Figure 4 predicts the further changes necessary to achieve an Ft of 300 GHz. Given this prediction it is expected that an Ft of 300 GHz would not require fundamental architectural change to the current device but only further optimization.

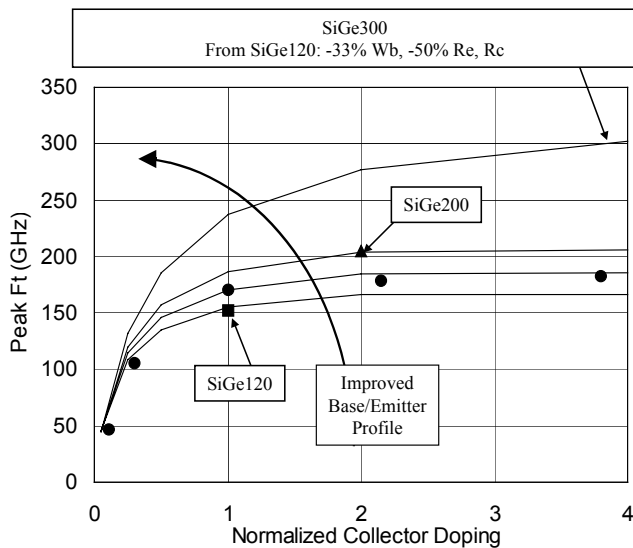


Figure 4: Peak Ft as a function of collector doping and base/emitter profile. Lines are predictions and represent increasingly aggressive base/emitter profiles. Solid symbols are experimental data points and specific data points for SiGe120, SiGe200 and what is predicted for SiGe300 are highlighted.

Integration of SiGe devices with advanced CMOS

As CMOS is scaled, thermal budget constraints of advanced bipolar devices and CMOS devices diverge leading to increased difficulty with integration. In this section we will report results of the successful integration of 200 GHz SiGe bipolar transistors with 0.13 μm generic CMOS. This result is obtained without changing the process flow sequence or architecture already employed in the integration of SiGe devices in 0.35 μm , 0.25 μm or 0.18 μm nodes.

In all these nodes, the CMOS gate, re-oxidation, LDD and pocket implants are performed prior to SiGe epi deposition and the source-drain implants and final anneal are performed after the SiGe bipolar transistor is completely formed. This helps to limit exposure of the SiGe transistor to CMOS related thermal budget from the gate and re-oxidation cycles. The drawback of this approach is that the LDD and pocket implants are in place during SiGe deposition which typically includes a high temperature bake to clean the surface.

We have built 0.13 μm CMOS in SiGe200 by limiting the SiGe bake temperature through improved pre-conditioning of the surface, proper re-optimization of the thermal budget between pre- and post- SiGe epitaxy and re-optimization of the transistor implants to center performance. The results of generic 0.13 μm CMOS integrated in SiGe200 are shown in Figure 5. Low-power and high-performance variants have also been demonstrated.

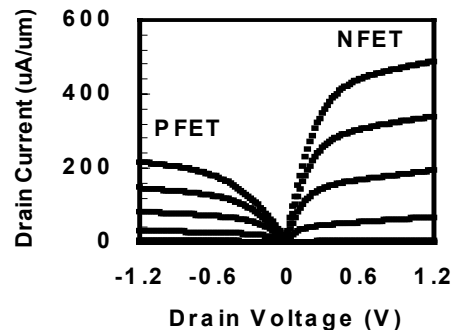
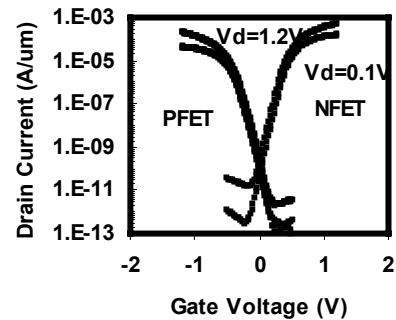


Figure 5: Generic 0.13 μm CMOS $I_d(V_g)$ and $I_d(V_d)$ characteristics when integrated with SiGe200.

Advanced Passive Elements

Integrated inductors require large die area and suffer from losses that limit their usefulness. Improving inductor performance is thus a major thrust of advanced RF technologies. A 6 μm thick top Al metal module has been developed to significantly improve inductor performance over that typical of 2-4 μm thick top metal without adding the process cost and complexity of additional thick Cu layers.

Figure 6 shows nearly a factor of 2 reduction in inductor area can be achieved at a fixed Q with a 6 μm thick top metal vs. use of more conventional 3 μm thick metal. While the exact area saving is a function of the inductor size and design, the die cost saving can in many cases more than offset the cost of the thicker metal module.

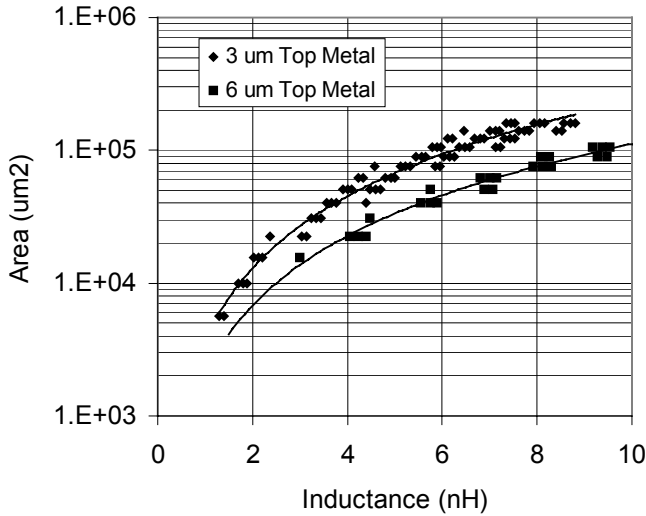


Figure 6. Inductor area as a function of inductance for a 4-turn inductor with peak Q of 10 built in 3 μm and 6 μm top metal respectively.

Capacitors also take up significant amount of die area and focus has been toward increasing their density. 2 fF/ μm^2 capacitors are now being introduced into production. By stacking 2 fF/ μm^2 capacitors higher capacitance density can be achieved. Figure 7 shows reliability data for a 2 fF/ μm^2 MIM capacitor which is capable of 5V operation and has a breakdown voltage of >20V.

Technology nodes and benchmark performance

Several SiGe technologies are available today from commercial foundries. To provide a flavor for these, we will next review specific examples from Jazz Semiconductor. Table 1 describes electrical specifications for three major technology nodes created from the components described in the first three sections of this paper: SiGe90, SiGe120 and SiGe200.

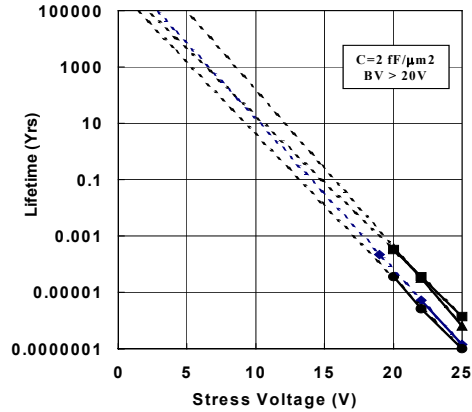


Figure 7. 2 fF/ μm^2 MIM capacitor constant stress lifetime. A lifetime of >1000 years is extrapolated for operation at 5V.

Table 1: Sample of optimized SiGe BiCMOS technology variants

		SiGe90	SiGe120	SiGe200
NPN	Ft (GHz)	78/38	150/78/38	200/80
	Fmax (GHz)	160/100	180/160/100	220/160
	BVceo (V)	3.5/6	2.3/3.5/6	2.0/3.5
CMOS	Vdd (V)	3.3	3.3/1.8	3.3/1.2
	Lmin (um)	0.25	0.18	0.13
Resistors	Rs (ohm/sq)	245/1000	245/25	245/25
Capacitor	C (fF/mm2)	2, 4	1	2, 4
Routing	# Layers	3, 4, 5	6	6
Top Metal	Thickness (um)	3, 6	3	3

SiGe90 is a low-cost process designed for the efficient integration of RF transceivers. SiGe90 includes 2 NPNs (78 and 38 GHz) as well as 3.3V CMOS. Metal options include 3 or 6 μm of top metal with three to five layers of metal. The very low base resistance of this self-aligned NPN leads to low noise figure and high gain at low currents as demonstrated by the LNA measurements shown in Table 2. Records for silicon-based technology in noise figure (0.99 dB) and power consumption (sub 3 mW) have been reported in single stage (3) and cascode (Bi-FET (4)) PCS-band LNAs built in SiGe90.

Table 2: SiGe90, 2 GHz, Packaged LNA measurements

	Ref (3)	Ref (4)	
Vcc	3	2.2	V
Ic	2.75	1.4	mA
IP3	12.6	6.5	dBm
Gain	16.2	16.0	dB
NF	0.99	1.67	dB
S11	-10	-10	dB
S22	-19	-12	dB

SiGe120 is a fully featured process designed for the efficient integration of 10 and 40 Gb/s transceivers. SiGe120 includes additional features such as higher levels of metal, a metal resistor for low losses to substrate and the addition of a 150 GHz NPN.

Figure 8 shows results of a highly integrated 10 Gb/s transceiver built in SiGe120 demonstrating very low jitter performance. The transceiver consumes only 1.9 W making it also one of the lowest power 10 Gb/s transceivers reported to date. Figure 9 compares jitter (as measured by inter-symbol-interference or ISI) simulated for a CML buffer built with SiGe120 and built with 0.13 μm CMOS (5). While acceptable performance can be achieved with 0.13 μm CMOS at 10 Gb/s for low fan-out, SiGe120 can result in dramatic improvements in ISI particularly for higher fan-out enabling higher performance and more design flexibility in achieving low power consumption (5).

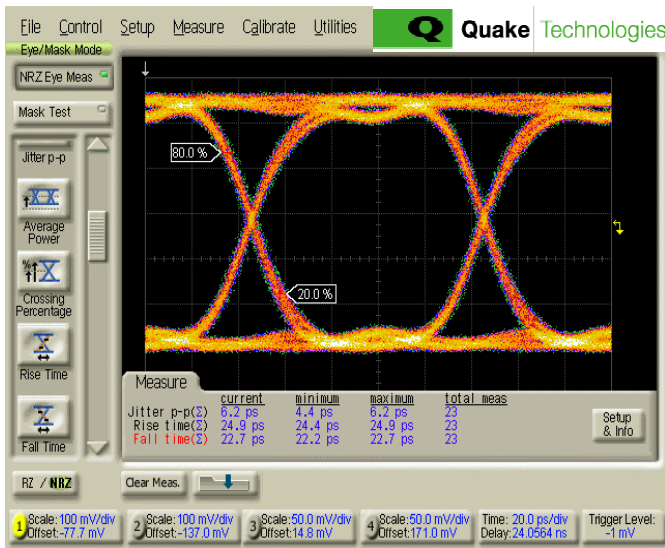


Figure 8. Eye diagram at 10.7 Gb/s. Rise/fall times are 23-25 ps and total jitter (on HP83480A DCA, with cables) is 6.2ps. Figure is courtesy of Quake Technologies.

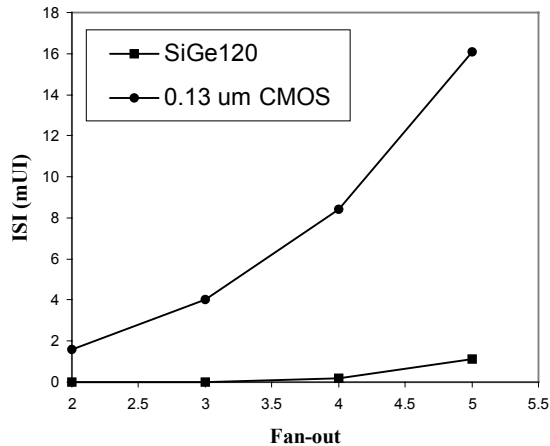


Figure 9. Inter-Symbol-Interference (ISI) as a function of fanout for a 10 Gb/s CML buffer simulated with SiGe120 and generic 0.13 μm CMOS respectively (5).

SiGe200 is a next generation process designed for 40 Gb/s communication systems and higher frequency wireless

applications. Figure 10 shows H21 and Unilateral gain extrapolated to an Ft and Fmax of 205 and 210 GHz respectively.

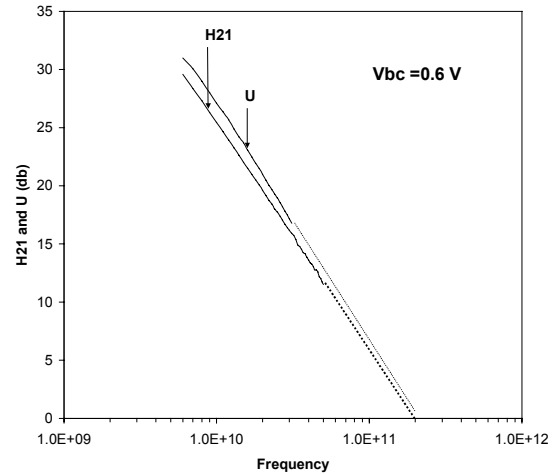


Figure 10. H21 and unilateral gain vs. frequency extrapolated to Ft of 205 GHz and Fmax of 210 GHz.

Conclusion

SiGe BiCMOS is fast becoming the technology of choice for the realization of cost effective wireless and wire-line transceivers.

In this paper, we have reviewed advances in SiGe bipolar device performance demonstrating Ft and Fmax in excess of 200 GHz and have predicted a path for achieving performance in excess of 300 GHz. In this paper we have also reported the successful integration of 0.13 μm generic CMOS with >200 GHz SiGe. Finally, we have reviewed optimized SiGe BiCMOS technology nodes available at a commercial foundry and described some record breaking circuit results including the realization of PCS band LNAs with the lowest noise figure and lowest power consumption reported to date for silicon based devices and an ultra low power, low jitter 10 Gb/s transceiver.

Acknowledgements

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