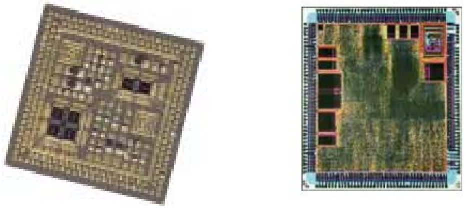
Jazz Semiconductor IC Technologies Enabling Advanced Analog and RF SiP Designs

David Cheskis – Technical Marketing Manager, Jazz Semiconductor

Introduction

Jazz Semiconductor has developed Si CMOS and SiGe BiCMOS technologies that change the way communications systems are designed and partitioned. Jazz now offers several different technology modules that allow the analog partition of a system to include high speed, high performance and high voltage blocks integrated as part of a System-in-Package (SiP) configuration.

The System-in-Package offers an alternative to the challenges involved with integrating both analog and digital functions into a System-on-Chip (SoC) design. The SiP approach allows the system designer to implement the analog and digital partitions into technologies optimized for those unique functions. The digital components can be integrated into high performance CMOS while the analog and RF blocks are implemented in lower cost high voltage CMOS, RF CMOS and high performance SiGe BiCMOS. Examples of the SiP and SoC are shown below and demonstrate the die size and integration requirements.



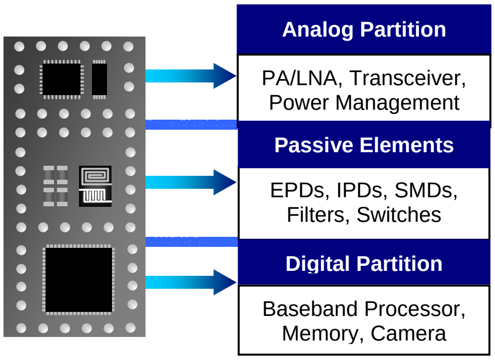
SiP **vs.** **SoC**

To accommodate the SiP designs, Jazz technologies are compatible with RF SiP design flows. This enables the system designer to optimize the cost and performance trade-offs necessary for high volume communications products. Together, this affords the system designer the opportunity to improve the system performance by optimizing individual system components and including the effects of the package or substrate. This chip and package co-development is a significant advance in the design and implementation of communication ICs.

System Partitioning

The SiP approach to system design is becoming more important as larger sections, and more functionality, become integrated into one mixed-signal product. When additional features are integrated into one IC, it becomes more difficult to accomplish that integration with a single technology, as in a System-on-Chip (SoC) design. The SiP allows for the system to be partitioned into separate analog and digital functions, so that each can be optimized separately for best performance.

The following diagram shows an example of SiP partitioning. A typical wireless system includes analog and RF blocks such as the PA, LNA, VCO, PLL, ADC, integrated passives, and power management. The digital partition includes baseband processing, memory, camera processing and other digital functions. Applying the SiP design approach allows each of these partitions to be individually optimized for performance and cost. It also affords IP re-use and reduces time-to-market. Employing the optimal IC technology for each system partition is key to realizing these advantages and allows the analog components to scale even when more advanced digital processes are employed.



Analog Scaling

The SiP approach allows the designer to take full advantage of both increased digital density and analog scaling. Advanced digital CMOS scales according to Moore's Law; increasing the digital density by approximately 50% in each generation. Unfortunately, the analog and passive devices do not achieve similar performance improvements in subsequent CMOS generations. In fact, Design-for-Manufacturing (DFM) issues in advanced digital technology nodes present additional challenges in shrinking the analog blocks. The Jazz technology roadmap has aggressively scaled the passive components (MIM, inductor, etc.) along with scaled CMOS and HBT devices in analog technologies. System partitioning allows the designer to take advantage of this analog scaling by utilizing the appropriate technology for each block and effectively scaling both the analog and digital content.

Analog scaling and system partitioning provide significant cost savings in several areas. Using analog technologies reduces cost due to the smaller die size and lower wafer and mask costs. Wafer and mask costs are reduced by using a larger geometry analog technology (180 nm vs. 90 nm) with equivalent or better analog/RF performance. SiP can provide the best IC cost structure when analog blocks aren't forced to consume expensive leading edge CMOS real estate.

Analog blocks can also be scaled because analog processes are also better-suited for noise isolation, which improves system performance while reducing die size. Substrate noise can be significantly reduced between analog blocks using a deep n-well process (triple well). This allows the IC layout to be more compact without concern for deteriorated performance. The system partitioning approach also provides an additional level of noise isolation by removing the noisy digital blocks from the same substrate as the sensitive analog circuitry. In addition to providing less cross-talk than in an SoC, the BiCMOS technology module allows designers to capitalize on the low noise performance of the HBT. Typically, analog performance that requires 90 nm CMOS can be achieved in 180 nm BiCMOS, again at smaller die sizes and lower die cost.

System partitioning also allows for optimized digital blocks with smaller area and lower cost. Using the proper digital technology also allows the IC designer to optimize the power dissipation of large digital blocks. When forced to utilize a digital technology in an analog block, designers are at the mercy of high leakage currents, high stand-by power and high power consumption. This can be mitigated in the SiP by choosing the appropriate technology for the digital sections without concern for the analog/RF performance.

Another important issue in SoC design is thermal management. In order to accommodate the analog and digital functions on one SoC chip, the die sizes have grown very large and present significant thermal challenges. By partitioning the system in the SiP, the thermal requirements of each chip can be addressed individually. This provides lower package cost and better reliability in the SiP implementation.

Even as all of these design constraints are managed in an SoC, the system designer still needs to be concerned with the package cost and performance. Using an RF SiP design flow, the system designer can determine the effects that the package and substrate will have on product performance. This approach allows the designer to control all aspects of the system performance, including where it is most efficient to partition the system between the analog and digital domains. Control over the ultimate system performance improves the yield and manufacturability of these advanced, highly integrated communications systems products.

Jazz Analog IC Technologies

Jazz continues to develop technologies that promote analog integration of system functions, including Si CMOS and SiGe BiCMOS from 0.5 µm to 130 nm, complete with high voltage operation up to 12 V. This allows for advanced integration of power management and other high voltage circuits onto the same system partition as high speed, high performance analog functions. Table 1 shows the Jazz analog technology modules.

Table 1: Jazz Technology Modules

0.5 µm	CMOS, RFCMOS, BCD
0.35 µm	60 GHz SiGe BiCMOS
0.25 µm	CMOS, RFCMOS, HV CMOS
180 nm	CMOS, RFCMOS, HV CMOS 90/120/200 GHz SiGe BiCMOS
130 nm	CMOS, RFCMOS 100/150/200 GHz SiGe BiCMOS

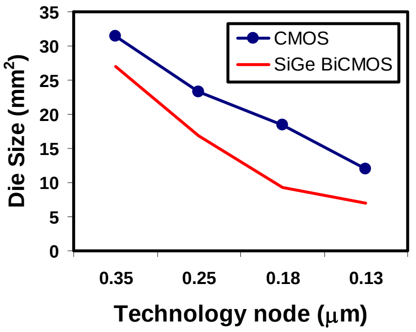
These extensive analog technology offerings enable integration of diverse components such as transceivers, amplifiers, ADC and power management into the analog partition of the system.

Highly efficient analog integration is also facilitated by the advanced passive elements in the Jazz technology modules. High density MIM capacitors, high Q inductors and triple n-well processes all allow for more compact designs at high speeds with improved performance. Each of these elements can be utilized where appropriate for cost and performance requirements as a result of the Jazz modular technology approach. Table 2 shows some of the passive element modules that are available in the Jazz technologies.

Table 2: High Performance Passive Elements

Device	Feature
MIM capacitor	5.6 fF/µm^2
Inductor (Q @ 2.4 GHz)	>25
Inductor thickness	3.0 – 6.0 µm

The effects of analog scaling using these technologies can be dramatic. The following chart shows the result of analog scaling on die size for various technology nodes, assuming nearly equal digital and analog content. The impact of analog scaling, including highly integrated passive devices, is to reduce the SiGe BiCMOS chip size compared to a digital CMOS implementation by 20 – 50 %. Along with this reduction in die size come lower die cost, reduced complexity and lower overall system cost.



With all of these pieces of the analog puzzle, Jazz has consolidated analog technologies that provide solutions for analog integration in one specialty foundry. This approach complements the advanced CMOS processes at 90 nm and 65 nm which are ideal for highly integrated digital functions. While these digital processes are capable of analog integration, they are not as cost effective, or of comparable performance, as 180 nm RFCMOS or 180 nm SiGe BiCMOS. Jazz specialty technology is complementary to advanced CMOS when a SiP design approach is applied, using analog and digital partitions optimized in an RF SiP design tool.

Conclusion

The SiP design approach is a more cost effective system solution than the SoC. It allows the designer to choose technologies optimized for specific analog functions that are lower cost than an SoC implementation. System partitioning also allows for shorter design cycles because each block utilizes the optimum technology, leading to lower development costs and faster time-to-market.

Jazz provides the technologies needed for analog functional integration in advanced communications systems. With high speed and high voltage modular technology offerings, most of the analog functions can be optimized on a single analog IC. Jazz technologies are compatible with the RF SiP flow and allow the system designer to take full advantage of analog integration and system partitioning.